



V Semester B.C.A. Degree Examination, Nov./Dec. 2016  
(CBCS – Fresh – 2016 – 17 & Onwards)  
BCA – 503 : COMPUTER ARCHITECTURE

Time : 3 Hours

Max. Marks : 100

**Instruction :** Answer *all* Sections.

## SECTION – A

- I. Answer **any ten** questions. **Each** carries **two** marks. (10×2=20)
- 1) What is Computer Architecture ? 2
  - 2) State and prove DeMorgan's theorem. 2
  - 3) Mention the different logic families of IC. 2
  - 4) Distinguish between RAM and ROM. 2
  - 5) What is Parity bit ? 2
  - 6) Write the BCD code for decimal number 8745.42<sub>(10)</sub>. 2
  - 7) What are the two types of control organization ? 2
  - 8) Define program counter. 2
  - 9) Mention the major components of CPU. 2
  - 10) What is PSW ? 2
  - 11) What is Polling ? 2
  - 12) What is memory management system ? 2

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## SECTION – B

- II. Answer **any five** questions. **Each** carries **five** marks. (5×5=25)
- 13) Prove NAND and NOR gates as universal gates. 5
  - 14) Explain PIPO shift Register with a diagram. 5
  - 15) Discuss the Parity generator and Parity checker. 5
  - 16) Explain the operation of interrupt cycle with a flow chart. 5

P.T.O.



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|---|---|
| 17) Explain input-output instructions.  | 5 |
| 18) Explain the three types of CPU organization.  | 5 |
| 19) Explain the source initiated data transfer using handshaking with a block diagram and timing diagram. | 5 |
| 20) Write a note on memory hierarchy in a computer system.  | 5 |

## SECTION – C

III. Answer **any three** questions. **Each** carries **fifteen** marks. **(3×15=45)**

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|---|----|
| 21) a) Define K-Map ? Simplify the following Boolean function using K-Map :<br>$F(A, B, C, D) = \sum(0, 2, 4, 6, 10, 11, 12, 13, 14, 15)$ | 8  |
| b) Explain different binary codes.  | 7  |
| 22) a) Define counter. With a neat diagram explain 4-bit synchronous binary counter.  | 8  |
| b) Explain octal to binary encoder with diagram.  | 7  |
| 23) Explain the design of basic computer with flow chart.   | 15 |
| 24) What is addressing mode ? Explain the different types of addressing modes with examples.  | 15 |
| 25) a) Explain DMA controller with a block diagram.   | 7  |
| b) Explain the working of associative memory.   | 8  |

## SECTION – D

IV. Answer **any one** question. **Each** carries **ten** marks. **(1×10=10)**

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|--|---|
| 26) a) Explain the working of full adder.  | 5 |
| b) Write a note on modes of data transfer. | 5 |
| 27) a) Explain the common bus system.      | 5 |
| b) Write a note on RISC and CISC.          | 5 |
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